

VACUUM FLUORESCENT DISPLAY  
MODULE  
SPECIFICATION

MODEL : GU128X32-311  
CUSTOMER : MAGELLAN

SPECIFICATION NO. : DS-493-0000-04

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1. SCOPE This specification covers the requirement of vacuum fluorescent graphic display module, model: GU128x32-311.

## 2. General description

This display module consists of 128X32 dots Vacuum Fluorescent Display, high voltage drivers controller refresh memory and DC/DC convertor.

## 3. Absolute Maximum Ratings

	Symbol		Unit
Power supply voltage	Vcc	+7.0	VDC
High level input voltage	VIH	Vcc1	VDC
Low level input voltage	VIL	-0.5	VDC

## 4. Electrical Ratings

	Symbol	Min.	Typ.	Max.	Unit	Condition
Low level input voltage	Vcc	4.75	5.00	5.25	VDC	-
High level input voltage	VIH	2.2	-	Vcc	VDC	Vcc=5.0VDC
Low level input voltage	VIL	0	-	0.8	VDC	Vcc=5.0VDC
Power supply current	Icc	-	950	1300	mADC	Vcc=5.0VDC ALL dots ON

Power rising time must be less than 20ms.

Power supply current might be double of the above value at power-on rush time.

## 5. Optical Ratings

Dot Formation	:	128x32 dot
Dot Size	:	0.45 mm x 0.45 mm (XxY)
Dot Pitch	:	0.65 mm x 0.65 mm (XxY)
Active Display Area	:	83.0 mm x 20.6 mm (XxY)
Luminance	:	400 fL (Min.) 660 fL (Typ.)
	:	Life : 5000hrs. (For half brightness)
Color	:	Blue green

## 6. Environmental Conditions

Operating Temperature	:	-40 ~ 85 °C
Storage Temperature	:	-50 ~ 85 °C
Operating Humidity	:	20 ~ 85 % (No condensation)

## 7. Mechanical Test Condition

Vibration	:	55 ~ 500 Hz, 14.7m/s <sup>2</sup> 3 directions, 30min. each
Shock	:	980m/s <sup>2</sup> 9ms 3 directions

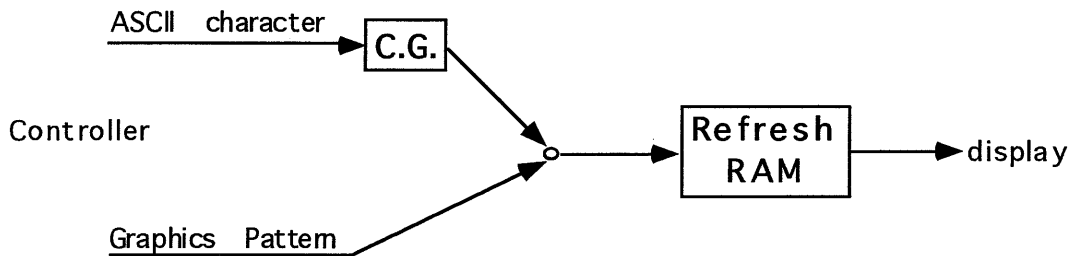
8 Function

This module provides the function of 8bit parallel Date Write.  
 Available character fonts are listed on the page8 and 9.  
 A date write is done during Busy line is low.

*WR	Function	Bus Direction
↓	Data Write	Host → Module

8.1 Software module

This display module has one refresh RAM. Each refresh RAM maintain one screen size display image. Either RAM is selected to send a image to the display.  
 This display module accepts blocks of data to control module and write characters or graphics image into the refresh RAM.



C.G. character Generator

8.2 Structure of data block

A data block consists of " Header " , " Op Code " and " Data " .

" Header " + " Op Code " + " Data "

01 Hex      1Byte

" Header " : 01 Hex

" Op Code " : Operation Code which specify a type of " Data " such as Graphics, character and command

" Data " : Data block

8.3 Op Code

8.3.1 Character write Op Code : " C "

Format

(01Hex) + (" C " 43 Hex) + Start ADRS + LEN + Write Mode

1 Byte      1 Byte      1 Byte

+ chr(1) + chr(2) + ... + chr(LEN)

Description

Write ASCII characters into refresh RAM which is selected by command.

" Chr(1) is stored at " start ADRS ".  
 " Chr(2) is stored at " start ADRS + 1  
 In case the location over the refresh RAM size,  
 next position is left end next lower line.

(Adrs 00H)					
				(start adrs) chr(1)	chr(2)
chr(3)	...	chr(LEN)			

Write Mode

Display image (character Font Pattern) can be combined with Data in refresh RAM before stored into refresh RAM.

- " A " : RAM ← RAM .And. Chr Font
- " O " : RAM ← RAM .Or. Chr Font
- " E " : RAM ← RAM .Exor. Chr Font
- " S " : RAM ← Chr Font (Just Store)

8.3.2 Graphic Write Vertical Op Code : " G " 47Hex

Format

01 Hex + ( " G " 47 Hex) + Start ADRS + LEN + Write Mode  
2 Byte      2 Byte      1 Byte  
 + PT(1) + PT(2) + ... + PT(LEN)  
Graphic pattern

Description

Write Bit map pattern into refresh RAM which is selected by command.

PT(1) is stored at " start Adrs ".  
 PT(2) is stored at " start Adrs + 1 ".  
 In case the location over the refresh RAM  
 size  
 next position is Address " 00Hex ".

				PT(4)	
			(start adrs) PT(1)	:	
			PT(2)	PT(LEN)	
			PT(3)		

Write Mode

Display image (Bit map Pattern) can be combined with Data in refresh RAM before stored into refresh RAM.

- " A " : RAM ← RAM .And. PT
- " O " : RAM ← RAM .Or. PT
- " E " : RAM ← RAM .Exor. PT
- " S " : RAM ← PT (Just Store)

8.3.3 Graphic Write Horizontal Op Code : " H " 48 Hex

Format

01 Hex + ( " H " 48Hex) + Start ADRS + LEN + Write Mode  
2 Byte      2 Byte      1 Byte  
 + PT(1) + PT(2) + ... +PT(LEN)  
Graphic pattern

Description

Write Bit map pattern into refresh RAM which is selected by command.

- PT(1) is stored at " start Adrs ".
- PT(2) is stored at " start Adrs + 4 ".

( In case the location over the refresh RAM size  
 next position is left end of next lower Row. )

	PT(1)	PT(2)	→ PT(N)
PT(NH) →			→ PT(LEN)

Write Mode

Display image (Bit map pattern) can be combined with Data in refresh RAM before stored into the RAM.

- " A " : RAM ← RAM .And. PT
- " O " : RAM ← RAM .Or. PT
- " E " : RAM ← RAM .Exor. PT
- " S " : RAM ← PT (Just Store)

8.3.4 Control Code

Format

01 Hex + " 0 " 4F Hex + "command code"  
1 Byte

Description

Command Code	Function
" P "	Clear refresh RAM
" Q "	Quick write
" R "	Flicker less
" S "	Display off
" T "	Display on (Default)
" 0 "	Select Character Table 0 (Default)
" 1 "	Select Character Table 1

Luminance Control

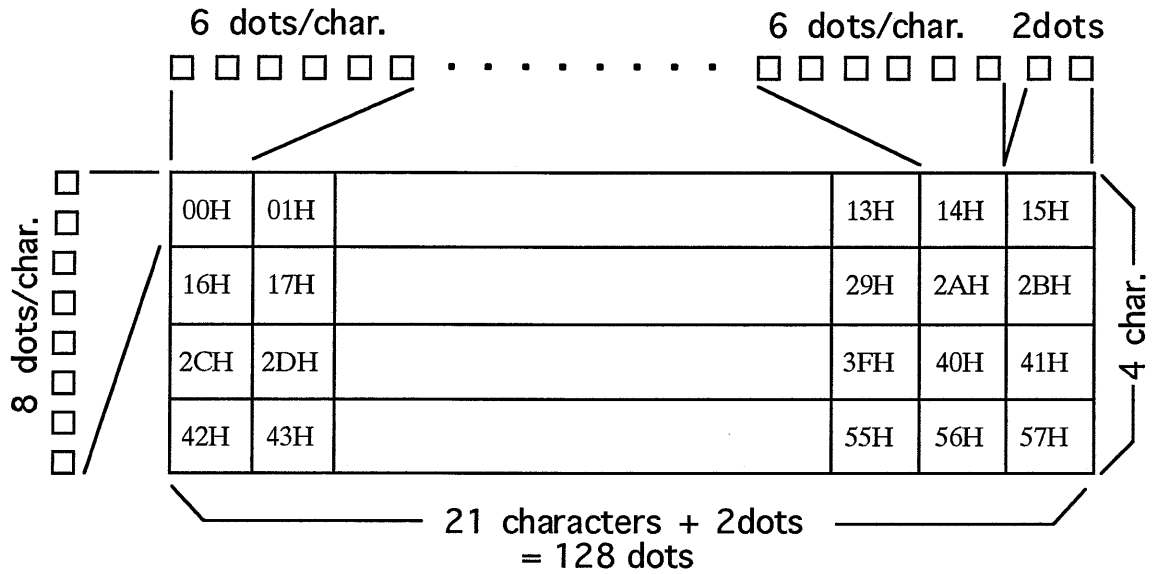
Command Code	Luminance	Command Code	Luminance
" a "	100%	" i "	17%
" b "	81%	" j "	14%
" c "	65%	" k "	11%
" d "	52%	" l "	9%
" e "	42%	" m "	7%
" f "	33%	" n "	5%
" g "	27%	" o "	4%
" h "	21%	" p "	3%

8.4 Blanking

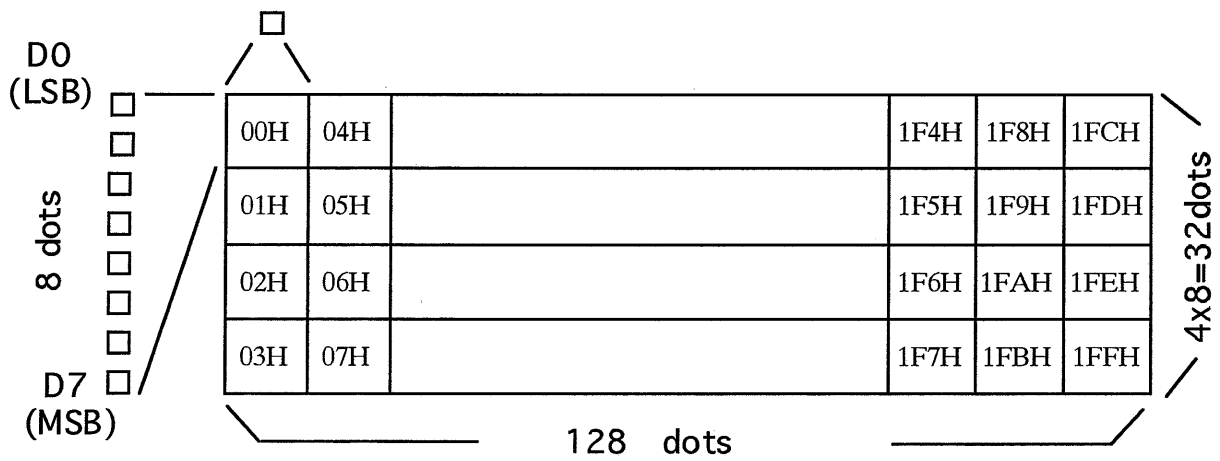
Display will be blanked by BL= " 0 " . There are no change in the RAM during blanking, previous will be recovered by BL= " 1 " .

8.5 Writing Position

A) Character Data Writing Position



B) Graphic Data Writing Position



1 : Turn on  
0 : Turn off

8.6 Character Table

The following 2 character tables are selected by command (see page 8.3.4)

8.6.1 International character

	D7	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1			
	D6	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1			
	D5	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1			
	D4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1			
D3	D2	D1	D0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	Å	Ä		0	á	ä	å	ä	å	ä	å	ä	å	ä	å	ä	å	ä
0001	1	Å	Ä	!	1	á	ä	å	ä	å	ä	å	ä	å	ä	å	ä	å	ä
0010	2	Å	Ä	"	2	á	ä	å	ä	å	ä	å	ä	å	ä	å	ä	å	ä
0011	3	Å	Ä	#	3	á	ä	å	ä	å	ä	å	ä	å	ä	å	ä	å	ä
0100	4	Å	Ä	\$	4	á	ä	å	ä	å	ä	å	ä	å	ä	å	ä	å	ä
0101	5	Å	Ä	%	5	á	ä	å	ä	å	ä	å	ä	å	ä	å	ä	å	ä
0110	6	Å	Ä	&	6	á	ä	å	ä	å	ä	å	ä	å	ä	å	ä	å	ä
0111	7	Å	Ä	'	7	á	ä	å	ä	å	ä	å	ä	å	ä	å	ä	å	ä
1000	8	Å	Ä	(	8	á	ä	å	ä	å	ä	å	ä	å	ä	å	ä	å	ä
1001	9	Å	Ä	)	9	á	ä	å	ä	å	ä	å	ä	å	ä	å	ä	å	ä
1010	A	Å	Ä	*	:	J	Z	j	z	J	Z	j	z	J	Z	j	z	J	Z
1011	B	Å	Ä	+	:	K	L	k	l	K	L	k	l	K	L	k	l	K	L
1100	C	Å	Ä	,	<	L	\	l		L	\	l		L	\	l		L	\
1101	D	Å	Ä	-	=	M	I	m	)	ö	ö	ö	ö	ö	ö	ö	ö	ö	ö
1110	E	Å	Ä	.	>	N	^	n	˘	ö	ö	ö	ö	ö	ö	ö	ö	ö	ö
1111	F	Å	Ä	/	?	O	_	o		ö	ö	ö	ö	ö	ö	ö	ö	ö	ö

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8.6.2 CUSTOM character

	D7	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1			
	D6	0	0	0	0	1	1	1	1	0	0	1	0	1	1	1			
	D5	0	0	1	1	0	0	1	1	0	1	1	0	1	1	1			
	D4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1			
3210	DDDD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		
0000	0				0	a	P	`	P	.	o	'	:o	o	h	L		·	¶
0001	1			!	1	A	Q	R	o	.	1	'	:1	1	h	L		·	¶
0010	2			"	2	B	R	E	R	.	2	'	:2	2	h	L		·	¶
0011	3			#	3	C	S	c	S	.	3	'	:3	3	h	L		·	¶
0100	4			\$	4	D	T	D	T	.	4	'	:4	4	h	L		·	¶
0101	5			%	5	E	U	E	U	.	5	'	:5	5	h	L		·	¶
0110	6			&	6	F	V	F	V	.	6	'	:6	6	h	L		·	¶
0111	7			'	7	G	W	G	W	.	7	'	:7	7	h	L		·	¶
1000	8			(	8	H	X	H	X	.	8	'	:8	8	h	L		·	¶
1001	9			)	9	I	Y	I	Y	.	9	'	:9	9	h	L		·	¶
1010	A			*	:	J	Z	J	Z	.	A	'	:A	A	h	L		·	¶
1011	B			+	:	K	[	K	[	.	B	'	:B	B	h	L		·	¶
1100	C			,	<	L	\	L		.	C	'	:C	C	h	L		·	¶
1101	D			-	=	M	]	M	)	.	D	'	:D	D	h	L		·	¶
1110	E			.	>	N	^	N	~	.	E	'	:E	E	h	L		·	¶
1111	F			/	?	O	_	O	~	.	F	'	:F	F	h	L		·	¶

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## 8.7 Data processing and Command Execution time

(The figure in this table are reference only.)

Op Code & Function	Quick Write Mode			Flickerless Mode
	1st Byte	2nd ~ 5th Byte	6th Byte ~	
" C " Char. Write	40 $\mu$ s	45 $\mu$ s	75 $\mu$ s	See Note 1

Op Code & Function	Quick Write Mode			Flickerless Mode
	1st Byte	2nd ~ 7th Byte	8th Byte ~	
" G " Graphic Write " H "	40 $\mu$ s	45 $\mu$ s	50 $\mu$ s	See Note 1

Op Code & Function	Quick Write Mode		Flickerless Mode
	1st & 2nd Byte	3rd Byte	
" P " CLR. RAM	40 $\mu$ s	500 $\mu$ s	See Note 1
" Q " Quick WR	40 $\mu$ s	45 $\mu$ s	
" R " Flickerless	40 $\mu$ s	45 $\mu$ s	
" S " Disp. OFF	40 $\mu$ s	50 $\mu$ s	
" T " Disp. ON	40 $\mu$ s	50 $\mu$ s	
Lumi. Control	40 $\mu$ s	55 $\mu$ s	
" 0 " Select. Chr. 0	40 $\mu$ s	40 $\mu$ s	
" 1 " Select. Chr. 1	40 $\mu$ s	40 $\mu$ s	

Note 1 Under the " Flickerless Mode ", Execution Time may be 2 to 4 times longer than Quick Write mode.

It is recommended to check the BUSY Line under Flickerless Mode.

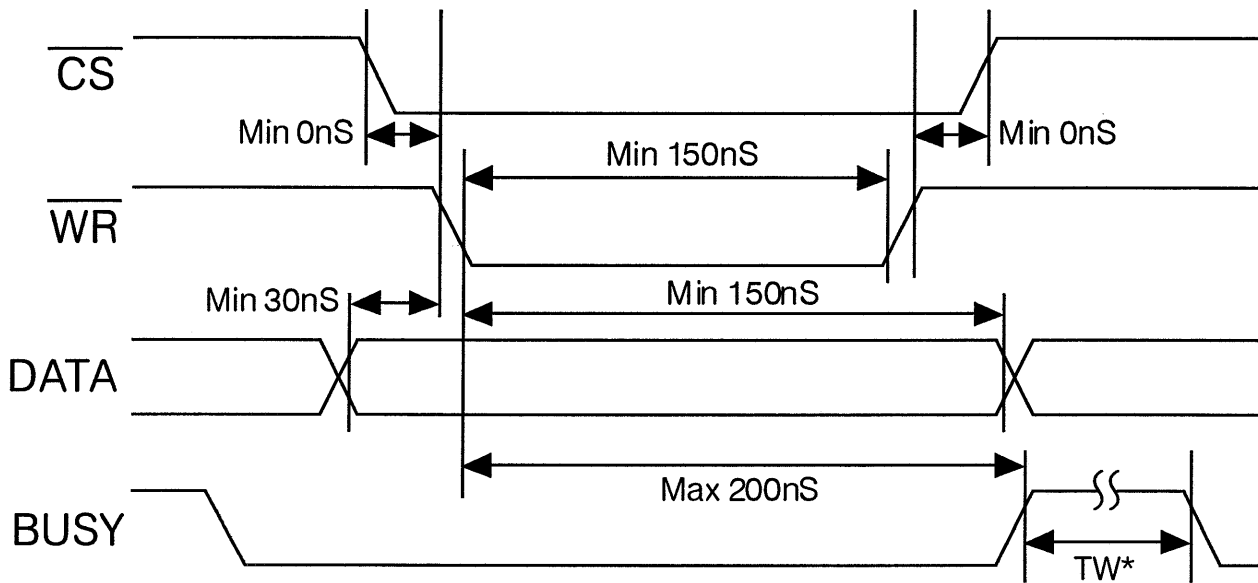
Note 2 Execution time is same as maximum of  $T_w$  (Busy Width).

## 9. Test Mode

Test Mode function is started when " T0 " is held at Low more than 100mSec. at power on.

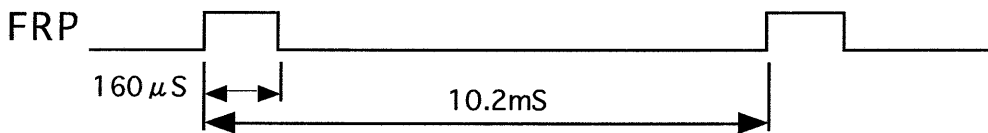
During Test Mode, all characters are displayed automatically and no any datas are accepted.

10. Timing  
10.1 Write Timing

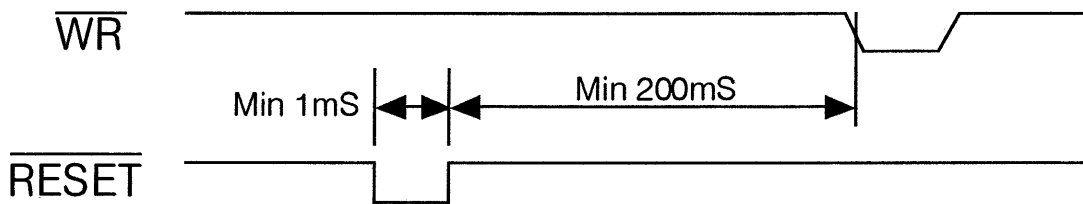


Tw : About 100  $\mu$  with most data or Commands.  
This figure will be confirmed on the specification.

10.2 FRP Timing

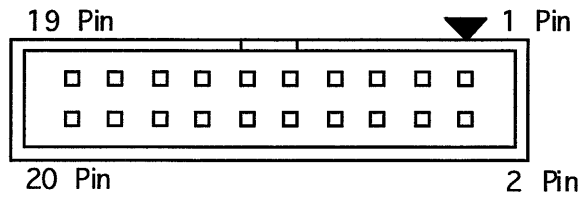


10.3 Reset Timing



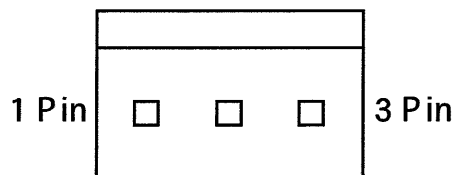
11. Pin Assignment

11.1 20pin data connector



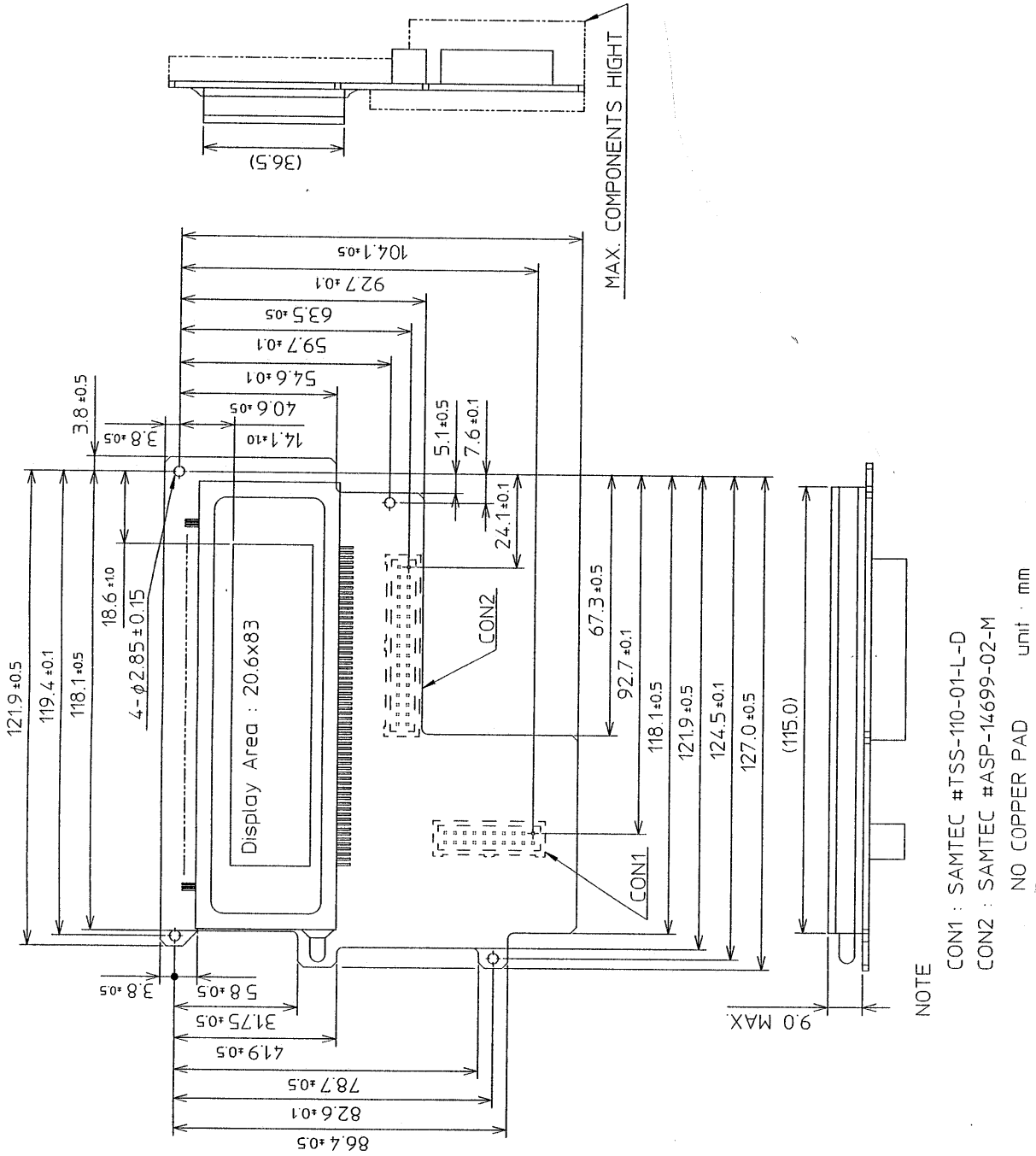
Pin No.	Signal	Pin No.	Signal
1	D7	2	D6
3	D5	4	D4
5	D3	6	D2
7	D1	8	D0
9	*WR	10	BUSY
11	*BL	12	FRP
13	GND	14	GND
15	+5V	16	+5V
17	GND	18	GND
19	*CS	20	*RESET

11.2 3pin power connector

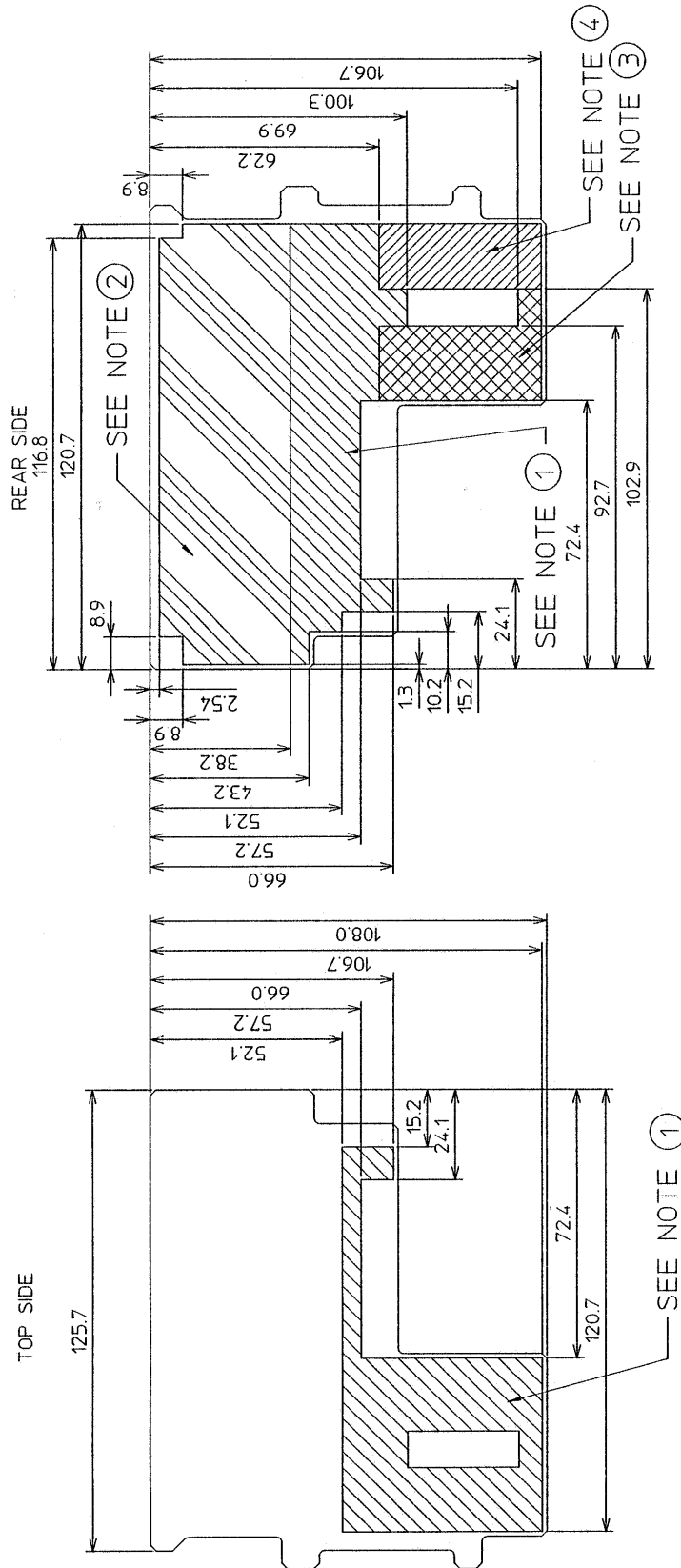


Pin No.	Description
1	+5V (Vcc)
2	T0
3	GND

12. Outline dimension 1



12. Outline dimension 2  
(Components height)



unit : mm

- ④ COMPONENT HEIGHT REAR SIDE 16.5 MAX.
- ③ COMPONENT HEIGHT REAR SIDE 4.5 MAX.
- ② COMPONENT HEIGHT REAR SIDE 6.3 MAX.
- ① COMPONENT HEIGHT TOP SIDE 5.0 MAX.

## IMPORTANT PRECAUTIONS

- \* All VFD Modules contain MOS-LSIs or ICs. Anti-Static handling are always required.
- \* V.F.Display consist of Soda Lime glass. Heavy shock more than 40G, thermal shock greater than 10°C/Minutes, direct hit with hard material to the glass surface -- especially to the EXHAUST PIPE may CRACK the glass.
- \* Do not push the display strongly. At mounting to the system frame, slight gap between display glass face and front panel is necessary to avoid a contact failure of lead pins of display. Twist or warp mounting will make a glass CRACK around the led pin of display.
- \* Neither DATA CONNECTOR or POWER CONNECTOR should be connected or disconnected while power is applied. As is often the case with most subsystems, caution should be exercised in selectively disconnecting power within a computer based system. The module receive high logic on strobe lines as random signals on all data ports. **Removal of primary power with logic signals applied may damage input circuitry.**
- \* Stress more than specification listed under the Absolute Maximum Ratings may cause PERMANENT DAMAGE of the modules.
- \* +5Volts power line must be regulated completely since all control logic depend on this line. Do not apply slow start power. Provide sufficient output current power source to avoid trouble of RUSH CURRENT at power on.
- \* Do not place the module on the conductive plate right after power off. Due to big capacitors on the module, more than 1 min. of discharging time is required to avoid the failure caused shorting power line.